REMARKS

Claims 1-27 are pending in the present application.

Claims 12-23 are rejected under 35 U.S.C. §101 as being directed to non-statutory subject matter.

Claims 1, 9, 10, 24, 26, and 27 are rejected under 35 U.S.C. §103(a) as being unpatentable over "Generation of Interpretive and Compiled Instruction Set Simulators," by Leupers *et al.* ("Leupers") in view of U.S. Patent No. 7,107,580 to Zemach *et al.* ("Zemach").

Claims 2 and 5 are rejected under 35 U.S.C. §103(a) as being unpatentable over Leupers in view of Zemach, and further in view of U.S. Patent No. 4,794,522 to Simpson ("Simpson").

Claims 3, 4, 6-8, and 11 are rejected under 35 U.S.C. §103(a) as being unpatentable over Leupers in view of Zemach, further in view of Simpson, and further in view of U.S. Pub. No. 2005/0102493 by DeWitt, Jr. *et al.* ("DeWitt").

Claims 12-16, 18, 19, and 22-23 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,477,683 to Killian *et al.* ("Killian") in view of DeWitt.

Claim 17 is rejected under 35 U.S.C. §103(a) as being unpatentable over Killian in view of DeWitt, and further in view of U.S. Pub. No. 2003/0217248 by Nohl *et al.* ("Nohl").

Claims 20 and 21 are rejected under 35 U.S.C. §103(a) as being unpatentable over Killian in view of DeWitt, and further in view of U.S. Pub. No. 2005/0160402 by Wang *et al.* ("Wang").

Claim 25 is rejected under 35 U.S.C. §103(a) as being unpatentable over Leupers in view of Zemach, and further in view of DeWitt.

Claims 1, 3, and 12-24 are amended herein. It is respectfully submitted that no new matter has been added.

Reconsideration of the application as amended herein is respectfully requested.

REJECTIONS

Rejections under 35 U.S.C. §101

Claims 12-23 are rejected under 35 U.S.C. §101 as being directed to non-statutory subject matter. Claims 12-23 are amended herein to include "a system, comprising: a processor..." As amended, Claims 12-23 meet the requirements for patentability under 35 U.S.C. §101. Therefore, Applicants respectfully submit that the Examiner's rejections of Claims 12-13 under 35 U.S.C. §101 are overcome.

Rejections under 35 U.S.C. §103(a)

Claims 1, 10, 24, and 27 are rejected under 35 U.S.C. §103(a) as being unpatentable over Leupers in view of Zemach. Applicants respectfully traverse the rejections and submit that Claims 1, 10, 24, and 27 are patentable under 35 U.S.C. §103(a) over Leupers in view of Zemach for at least the following reasons.

Claim 1 is amended to recite:

> a template configured to implement the functionality of the original instruction... **the template is associated with an instruction class** that describes a set of instructions of the instruction set architecture having a common behavior, and **wherein the original instruction is contained in the instruction class**.

Claim 1, emphasis added. Leupers does not provide such a teaching. Leupers describes generating instruction set simulators from instruction set models. Leupers, 3. System Overview, pp. 340-341. An instruction set model extracted from a processor models consists of register transfer templates, and a register transfer template specifics the assignment of some value to a destination (register, memory, or I/O port). Leupers, Section 4, p. 341. When a machine program is read, a macro is generated for each register transfer template and the macro consists of calls to appropriate simulation functions. Leupers, Section 4.2, p. 341. Each instruction of the program is decoded by determining a set of register transfers to be simulated in the instruction. Leupers, Section 4.3 Instructions, p. 341. During simulation, control passes along through register transfer simulation macros until all of the register transfers in the program have completed. Leupers, Section 4.4, p. 341. In other words, Leupers describes breaking instructions down into one or more register transfers and generating a macro to simulate each register transfer. Leupers does not teach:

> a template configured to implement the functionality of the original instruction... **the template is associated with an instruction class** that describes a set of instructions of the instruction set architecture having a common behavior, and **wherein the original instruction is contained in the instruction class**.

Claim 1, emphasis added. Zemach does not provide such a teaching either. Zemach describes translating a sequence of target instructions on a host machine using a simulator. Zemach, col. 1, ll. 35-40. The simulator includes a binary translator to translate the target code into host machine code. Zemach, col. 1, ll. 41-48. The binary translator translates a sequence of target instructions and stores the translated code in a translation cache.

Zemach, col. 1, ll. 56-62. Once translated, a block of translated code may be executed on the host processor a number of times from the translation cache. *Id.* Zemach does not teach:

> a template configured to implement the functionality of the original instruction... **the template is associated with an instruction class** that describes a set of instructions of the instruction set architecture having a common behavior, and **wherein the original instruction is contained in the instruction class**.

Claim 1, emphasis added. Because neither Leupers nor Zemach, alone or in combination, teach or suggest all of the features of Claim 1, Applicants respectfully submit that Claim 1, and Claims 2-11 that depend from Claim 1, are patentable under 35 U.S.C. §103(a) over Leupers in view of Zemach.

Claim 10 depends from Claim 1, and Claim 1 recites:

> a template configured to implement the functionality of the original instruction... **the template is associated with an instruction class** that describes a set of instructions of the instruction set architecture having a common behavior, and **wherein the original instruction is contained in the instruction class**.

Claim 1, emphasis added. For the reasons discussed above regarding the rejection of Claim 1, neither Leupers nor Zemach provides such a teaching. Therefore, Applicants respectfully submit that Claim 10 is patentable under 35 U.S.C. §103(a) over Leupers in view of Zemach.

Claim 24 recites substantially similar limitations as recited in Claim 1, including:

> a template configured to implement the functionality of the original instruction... **the template is associated with an instruction class** that describes a set of instructions of the instruction set architecture having a common behavior, and **wherein the original instruction is contained in the instruction class**.

Claim 24, emphasis added. For the reasons discussed above regarding the rejection of Claim 1, neither Leupers nor Zemach provides such a teaching. Therefore, Applicants respectfully submit that Claim 24, and Claims 25-27 that depend from Claim 24, are patentable under 35 U.S.C. §103(a) over Leupers in view of Zemach.

Claim 5 is rejected under 35 U.S.C. §103(a) as being unpatentable over Leupers in view of Zemach, and further in view of Simpson. Applicants respectfully traverse the rejections and submit that Claim 5 is patentable under 35 U.S.C. §103(a) over Leupers in view of Zemach, and further in view of Simpson for at least the following reasons.

Claim 5 depends from Claim 1, and Claim 1 recites:

> a template configured to implement the functionality of the original instruction… **the template is associated with an instruction class** that describes a set of instructions of the instruction set architecture having a common behavior, and **wherein the original instruction is contained in the instruction class**.

Claim 1, emphasis added. For the reasons discussed above regarding the rejection of Claim 1, neither Leupers nor Zemach provides such a teaching. Simpson does not provide such a teaching either. Simpson describes selecting a customizing a template to perform the work of a target instruction on a host computer. Simpson, col. 2, ll. 5-15. Templates are selected based on the op-code of a target instruction, and each template is a series of host instructions which performs the function of the target instruction op-code. *Id.* In other words, Simpson describes a template associated a specific target instruction. Simpson does not teach:

> a template configured to implement the functionality of the original instruction… **the template is associated with an instruction class** that describes a set of instructions of the instruction set architecture having a

> common behavior, and **wherein the original instruction is contained in the instruction class**.

Claim 1, emphasis added. Because neither Leupers, Zemach, nor Simpson, alone or in combination, teach or suggest all of the features of Claim 1, Applicants respectfully submit that Claim 5 is patentable under 35 U.S.C. §103(a) over Leupers in view of Zemach and further in view of Simpson.

Claims 3, 4, 6-8, and 11 are rejected under 35 U.S.C. §103(a) as being unpatentable over Leupers in view of Zemach, further in view of Simpson, and further in view of DeWitt. Applicants respectfully traverse the rejections and submit that Claims 3, 4, 6-8, and 11 are patentable under 35 U.S.C. §103(a) over Leupers, in view of Zemach, further in view of Simpson, and further in view of DeWitt for at least the following reasons.

Claims 3, 4, 6-8, and 11 depend from Claim 1, and Claim 1 is amended to recite:

> a template configured to implement the functionality of the original instruction… **the template is associated with an instruction class** that describes a set of instructions of the instruction set architecture having a common behavior, and **wherein the original instruction is contained in the instruction class**.

Claim 1, emphasis added. For the reasons discussed above with regard to the rejections of Claim 1 and 5, the combination of Leupers, Zemach and Simpson does not provide such a teaching. DeWitt does not provide such a teaching either. DeWitt describes obtaining performance data in a data processing system. DeWitt, ¶[0003]. As a processor processing instructions, an instruction cache determines which instructions are associated with performance indicators. DeWitt, ¶[0074]. Signals associated with performance indicators are sent to a performance monitor unit. *Id.* DeWitt does not teach:

> a template configured to implement the functionality of the original instruction... **the template is associated with an instruction class** that describes a set of instructions of the instruction set architecture having a common behavior, and **wherein the original instruction is contained in the instruction class**.

Claim 1, emphasis added. Because neither Leupers, Zemach, Simpson, nor DeWitt, alone or in combination, teach or suggest all of the features of Claim 1, Applicants respectfully submit that Claims 3, 4, 6-8, and 11 are patentable under 35 U.S.C. §103(a) over Leupers in view of Zemach, further in view of Simpson, and further in view of DeWitt.

Claims 12-16, 18, 19, and 22-23 are rejected under 35 U.S.C. §103(a) as being unpatentable over Killian in view of DeWitt. Applicants respectfully traverse the rejections and submit that Claims 12-16, 18, 19, and 22-23 are patentable under 35 U.S.C. §103(a) over Killian in view of DeWitt for at least the following reasons.

Claim 12 is amended to recite:

> a template configured to implement the functionality of the original instruction... **the template is associated with an operation class**...**wherein the original instruction is contained in the operation class**.

Claim 12. Killian does not provide such a teaching. Killian describes automatically configuring a process by generating a description of a hardware implementation of the processor and a set of software development tools for programming the processor. Killian, col. 6, ll. 32-37. A configured definition of a target instruction set is developed from a standardized language. Killian, col. 6, ll. 50-65. Instructions are defined into a class, and each instruction in a class has the same format and operand usage. Killian, col. 16, ll. 14-20. An instruction semantic statement describes the behavior of one or more instructions. Killian, col. 16, ll. 40-50. Killian does not teach:

> a template configured to implement the functionality of the original instruction... **the template is associated with an operation class**...**wherein the original instruction is contained in the operation class**.

Claim 12. For the reasons described above with regard to the rejection of Claim 3, DeWitt does not provide such a teaching either. Because neither Killian nor DeWitt, alone or in combination, teach or suggest all of the features of Claim 12, Applicants respectfully submit that Claim 12, and Claims 13-23 that depend from Claim 12, are patentable under 35 U.S.C. §103(a) over Killian in view of DeWitt.

Claim 17 is rejected under 35 U.S.C. §103(a) as being unpatentable over Killian in view of DeWitt, and further in view of Nohl. Applicants respectfully traverse the rejection and submit that Claim 17 is patentable under 35 U.S.C. §103(a) over Killian in view of DeWitt, and further in view of Nohl for at least the following reasons.

Claim 17 depends from Claim 12, and Claim 12 recites:

> a template configured to implement the functionality of the original instruction... **the template is associated with an operation class**...**wherein the original instruction is contained in the operation class**.

Claim 12. For the reasons discussed above with regard to the rejection of Claim 12, neither Killian nor DeWitt provide such a teaching. Nohl does not provide such a teaching either. Nohl describes simulating a program by accessing a table of compiled instructions. Nohl, ¶[0019]. If compiled data for an instruction is not stored in the table, the instruction is compiled and data is stored in the table for it. *Id.* By storing compiled data in the table, the instruction need not be compiled again if the instruction is re-executed. *Id.* Compiled data includes information suitable for the simulator to execute the instruction. Nohl, ¶[0039].

Compiled data is made up of one or more operations and one or more parameters. Nohl, ¶[0041]. Nohl does not teach:

> a template configured to implement the functionality of the original instruction… **the template is associated with an operation class**…**wherein the original instruction is contained in the operation class**.

Claim 12, emphasis added. Because neither Killian, DeWitt, nor Nohl, alone or in combination, teach or suggest all of the features of Claim 12, Applicants respectfully submit that Claim 17 is patentable under 35 U.S.C. §103(a) over Killian in view of DeWitt and further in view of Nohl.

Claims 20 and 21 are rejected under 35 U.S.C. §103(a) as being unpatentable over Killian in view of DeWitt, and further in view of Wang. Applicants respectfully traverse the rejections and submit that Claims 20 and 21 are patentable under 35 U.S.C. §103(a) over Killian in view of DeWitt, and further in view of Wang for at least the following reasons.

Claims 20 and 21 depend from Claim 12, and Claim 12 is amended to recite:

> a template configured to implement the functionality of the original instruction… **the template is associated with an operation class**…**wherein the original instruction is contained in the operation class**.

Claim 12, emphasis added. For the reasons discussed above with regard to the rejection of Claim 12, neither Killian nor DeWitt provides such a teaching. Wang does not provide such a teaching either. Wang describes adding advanced instructions to a microprocessor. Wang, ¶[0008]. A processor generated using instruction extensions includes an instruction fetch unit to decode the advanced instructions added. Wang, ¶[0031]. Operation classes associated opcodes with operands, and opcodes determine the behavior of an instruction

including the opcode. Wang, ¶[0102]. Opcodes are used to determine hardware and software associated with an execution unit for the opcode. *Id.* Wang does not teach:

> a template configured to implement the functionality of the original instruction… **the template is associated with an operation class**…**wherein the original instruction is contained in the operation class**.

Claim 12, emphasis added. Because neither Killian, DeWitt, nor Wang, alone or in combination, teach or suggest all of the features of Claim 12, Applicants respectfully submit that Claims 20 and 21 are patentable under 35 U.S.C. §103(a) over Killian in view of DeWitt, and further in view of Wang.

Claim 25 is rejected under 35 U.S.C. §103(a) as being unpatentable over Leupers in view of Zemach, and further in view of DeWitt. Applicants respectfully traverse the rejection and submit that Claim 25 is patentable under 35 U.S.C. §103(a) over Leupers in view of Zemach, and further in view of DeWitt for at least the following reasons.

Claim 25 depends from Claim 24, and Claim 24 is amended to recite:

> a template configured to implement the functionality of the original instruction… **the template is associated with an instruction class** that describes a set of instructions of the instruction set architecture having a common behavior, and **wherein the original instruction is contained in the instruction class**.

Claim 24, emphasis added. For the reasons discussed above, neither Luepers, Zemach, nor DeWitt teach or suggest all of the limitations of Claim 24. Therefore, Applicants respectfully submit that Claim 25 is patentable under 35 U.S.C. §103(a) over Leupers in view of Zemach, and further in view of DeWitt.

Accordingly, Claims 1-27 meet the requirements for patentability under 35 USC 103(a).

CONCLUSION

In view of the foregoing, Applicants submit that Claims 1-27 are in condition for allowance. Should minor matters remain, the examiner is invited to contact the undersigned at (949) 567-6700.

Respectfully submitted,

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